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DYNAMIC EFFECTS OF AVALANCHE-GENERATED CARRIERS.(U)
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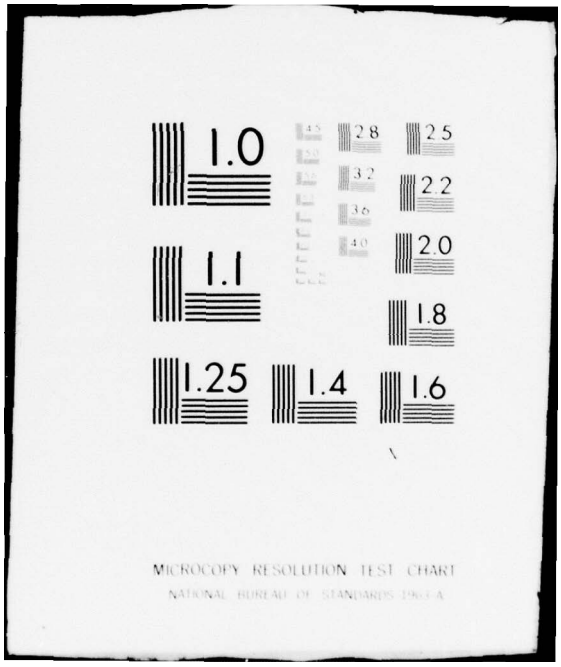
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DYNAMIC EFFECTS OF AVALANCHE-GENERATED CARRIERS

Final Scientific Report

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Dynamic effects of avalanche-generated carriers in transistors were investigated using a two-dimensional, time-domain computer program. Basic properties of MESFET logic devices were also studied.

The primary effect of avalanche process on bipolar transistor was found to be the majority carrier current in the lateral direction of the base creating a voltage drop opposite to the more usual edge-crowding effect. Avalanche multiplication in the

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Cont'd → stationary high field domain of a GaAs FET reduces device efficiency, but is usually not a destructive mechanism. Spontaneous avalanche in the gate-drain depletion region of the GaAs FET can spread to the drain and substrate leading to device failure.

The intrinsic switching frequency of a logic device could approach, but not exceed, f_T. In an IC, the switching speed depends mainly on g_m of the device and capacitive loading of the circuit. Nonuniformity in the device and circuit parameters up to 10% would not significantly affect IC performance.

DYNAMIC EFFECTS OF AVALANCHE-GENERATED CARRIERS

Abstract

Dynamic effects of avalanche process on bipolar and field-effect transistors were investigated via a two-dimensional time-domain computer program. Fundamental properties of GaAs and Si MESFET logic devices were also studied. The investigation of avalanche effects in bipolar devices ranged from weak avalanche multiplication (which could be used to improve device performance) to very strong spontaneous avalanche (which could result in second breakdown). All of these effects can be explained on the basis of avalanche-generated majority carrier flow in the lateral direction of the base.

The avalanche process in the GaAs FET could be initiated in the stationary high-field domain and/or the depletion region between the gate and the drain. The time constants of the avalanche are quite different in these two regions and produce different effects. Simulations of the Avalanche Memory Triode (AMT) indicated that in addition to possessing a dynamic memory the device has a switching speed several times faster than that of an equivalent bipolar transistor. However, high power dissipation makes the device not viable for large-scale IC applications.

The effort on logic device study was redirected to MESFETs (mainly GaAs FET). The intrinsic switching speed, optimum device, and operating parameters were investigated. It was found that under ideal conditions the switching frequency can approach, but not exceed, f_T.

Objectives and Efforts

The object of the study was to simulate the dynamic effects of avalanche-generated carriers on transistors and the avalanche memory triodes. The simulations were to be carried out using a two-dimensional time-domain computer program originally developed under Contract F44620-76-C-0043. Refinements on carrier transport in the computer program were to be made to improve computational stability under strong avalanche conditions. The efforts toward these goals are presented under subsections I. Refinements of computer program; II. Avalanche process in bipolar devices; III. Avalanche process in GaAs FETs; and IV. Simulation of high speed logic. A summary of new findings of this work is also given.

I. Refinements of Computer Program

In order to take advantage of the fast Fourier method [1] of solving Poisson's equation, it is necessary to solve the carrier transport equation explicitly. In this explicit technique, charge conservation and numerical stability are ensured by choosing a time increment Δt_t for updating the carrier transport sufficiently small such that $\Delta t_t \, v_{max} \leq \frac{\Delta X}{2}$, where v_{max} is the maximum carrier velocity and ΔX the grid size in the X direction. However, for computer economy, Poisson's equation is updated in a time increment $\Delta t_p > \Delta t_t$. The ratio $\Delta t_p / \Delta t_t$, an integer, ranges from two to twelve. Furthermore, the divergent and gradient operators are presented using a five-point scheme. This scheme allows the use of either forward or backward difference depending on the direction of carrier motion.

Another improvement on the program is the computation of the emitter and base junction voltage due to avalanche generated carriers. Previously, this voltage was only calculated in the junction itself. The new program includes two-dimensional hole current in the extrinsic base region and an external base resistance as shown schematically in Figure 1.

In connection with MESFET logic study a ring oscillator simulation program was created. The model for the ring oscillator is shown in Figure 2. In this model the device is characterized by the R-C time constant obtained from two-dimensional simulations and static I-V characteristics. The load capacitance, C, includes the device input capacitance obtained from the 2-D simulation and circuit loading. The drain I-V characteristics are scaled according to computer i_{DSS} (Figure 10). In this program, the physical parameters can be varied among devices in the ring oscillator; thus, the effects of nonuniformity in IC processing can be studied.

II. Avalanche Process in Bipolar Devices

Numerical results indicate that the primary effect of avalanche-generated carriers arises from the majority carrier lateral flow in the base. Such current produces a voltage drop which is opposite to the normal transistor base current. This hole feedback phenomenon (in n-p-n devices) can be divided into three regimes, i.e. the CATT regime, the AMT regime, and the second breakdown regime. The CATT regime has been reported previously.[2-8] Highlights on the results of the AMT and second breakdown are described here.

Similar to the CATT, the AMT[9] has a bipolar transistor-like structure with a hyperabrupt collector-base junction. The hole feedback voltage on the emitter-base junction can be self-sustaining after an input trigger signal. In this self-sustained state, the output current persists, i.e., the device possesses a dynamic memory. The memory can

be erased by an input trigger of opposite polarity to the "on" signal. A schematic AMT circuit and experimental input and output waveform are shown in Figure 3.

The positive feedback effect of the avalanche-generated hole current on the lateral potential distribution in the emitter-base junction is shown as a series of snapshots in Figure 4. This condition arises under a proper combination of the load and base to ground resistances. The computation becomes unstable when the current is large. In reality, the load resistance in the collector circuit will arrest the current growth by lowering the collector voltage and by reducing the avalanche hole generation. The "on" state is a dynamic equilibrium between the junction voltage and the hole current. This condition may be expressed in a one-dimensional approximation by $dV_{EB}/di_p < O$, where i_p is the hole current which generates the junction voltage. Numerical results also show that the hole feedback increases the g_m of the AMT over normal transistor by several times. This increase explains the faster switching speed of the device since the switching speed is related to the ratio $g_m/2\pi C$, where C is a total capacitance including circuit loading.

The AMT, in spite of its superior speed and its latching property, was found not to be viable for large-scale IC applications. The device requires a high-bias voltage (~15 V) and a minimum power dissipation of about 10 mW.

Computational results show that under strong avalanche conditions the collector-base junction of a transistor can behave like a TRAPATT. A high-field region is formed near the n^+ contact of the collector opposite the emitter, and another high-field region near the base remote from the emitter, as shown in the upper portion of Figure 5. These high-field regions sustain the avalanche process even though V_{CB} is reduced by the large current in the external load. The computer simulation shows a strong pinch-in[10] of the emitter-base junction voltage accompanying the TRAPATT behavior shown in the lower portion of Figure 5. It is noted that the model of the emitter base-junction in the computer program is not adequate for very high injection conditions. Thus, this pinch-in effect always leads to numerical instability. Nonetheless, these results suggest that second breakdown can be due to avalanche process independent of thermal effects.

It is believed that the TRAPATT-like behavior is, indeed, the primary mechanism for second breakdown with or without thermal effects. Experiment and computation show that a hyperabrupt junction such as that used in the CATT renders the device less vulnerable to TRAPATT actions, and second breakdown, therefore, is much less likely to occur. Experimentally, all the CATTs and AMTs operate safely without emitter ballast, in contrast to normal transitors.

III. Avalanche Process in GaAs FET

The avalanche process in GaAs FET according to numerical results can be initiated in two distinct regions. The time constants and consequences of the two can be quite different.

A time sequence of hole density buildup in the stationary high-field domain of the conducting channel is shown in Figure 6. As indicated in these snapshots, the time required to form a significant electron-hole pair density (>10% of N_D) is a small fraction of the rf period. This is because there are already a large number of mobile electrons in the channel and the carrier generation is usually due to single-pass avalanche multiplication. Since these carriers are generated during the peak of rf voltage, the process is dissipative and thus decreases device efficiency. However, the single-pass avalanche multiplicator is not a runaway process, and hence is not necessarily destructive.

Further time sequence frames showing both types of carriers in the gate-drain depletion region are shown in Figure 7. The carriers are generated near the gate where the electric field is highest. The avalanche spreads in two dimensions - toward the drain and toward the substrate, a normal one-sided gate structure. (Our simulation employs a symmetric gate structure for convenience.) The buildup time of the avalanche generated carriers to a level, say 10% of channel doping, is always longer in the gate depletion region than in the conducting channel's high-field domain. This is because the avalanche in the depletion region is initiated by a much smaller number of carriers emanating from thermal activation and/or leakage and is a multiple-pass electron-hole feedback process. This is a runaway process leading to device destruction unless checked by other nonlinear mechanisms or by an external means.

It is observed in the simulation of the FET under rf condition that in most cases the multiplication in the conducting channel occurs while the avalanche in the high-field region of the depletion layer remains negligible.

IV. Simulation of High-Speed Logic

Because the AMT was found not to be viable for large-scale IC, it was decided to investigate instead the basic properties of MESFET logic device since the time-domain progam is most suitable for this purpose. In addition, a ring oscillator simulator was also used in this study.

As reported previously,[11] a MESFET behaves like an RC circuit under impulse condition. To determine the impulse response, the drain current was computed for $t \geq 0$ while a time step voltage was applied to the gate at $t=0$. The gate voltage was set equal to pinch-off V_p and the drain voltage $V_D \geq |V_p|$. The i-t characteristics obtained were used to determine the device gain-bandwidth product, f_T, vs gate length, L. Effects of doping density were also studied since it is directly related to the optimum logic swing and the power-delay time product.

All i-t characteristics obtained show that f_T, even under velocity saturation condition, is determined by an R-C time constant. The usual velocity saturation gate transit time $\tau_T = L/v_s$ does not seem too meaningful in view of the numerical results. Physically, when the MESFET is subjected to the impulse input, the depletion region is enlarged to pinch off the drain current. The capacitance which determines the R-C constant arises from the amount of charge, ΔQ, displaced in the depletion region while the resistance is simply the channel resistance through which the charge flows.

The R-C or device time constant and f_T are determined from a semi-log plot of the i-t characteristic as shown in Figure 8. In this plot, the maximum current may be interpreted as the zero-gate bias saturation current i_{DSS}. Hence, the on-channel resistance may be estimated by the relation $r_D \approx |V_P| / i_{DSS}$, and the device input capacitance $C_{in} = \tau / r_D$. The f_T vs gate length for GaAs and Si MESFET are shown in Figure 9. It may be concluded that GaAs FETs are about twice as fast as that of Si in logic applications.

The quantities f_T, i_{DSS}, and V_P for a 2-μm gate GaAs FET vs doping density are shown in Figure 10. Note that f_T is independent of doping density. This is true because ΔQ is proportional to N_D while r_D is inversely proportioned to N_D. The pinch-off voltage and, hence, the optimum logic swing[12] ΔV is proportional to N_D. Thus, it appears that one can reduce the $P \cdot t_D$ product by reducing N_D without sacrificing switching speed. However, decreasing the logic swing would place stringent demands on uniformity in IC processing.

The intrinsic switching speed and the effect of circuit loading are studied by ring oscillator simulations. The voltage waveforms of a 5-stage, 1-μm gate inverter, with uniform devices and no parasitic capacitance, are shown in Figure 11. In Figure 11(a), the load resistors R_L are adjusted until $\Delta V = |V_p|$. In this case, the delay per stage is 35 ps. For TTL as used in Ref. (12), the minimum per stage would be twice as long, or 70 ps. According to simulation results, the minimum switching time per device per cycle is approximately $2\pi\tau$, i.e., the maximum switching frequency under ideal conditions is f_T. The delay per stage is increased when the logic swing is increased by increasing R_L or the bias voltage. The waveform for $V_p = 1.4\,\Delta V$ [Figure 11(b)] has a delay per stage of 45 ps (90 ps for TTL). The increase in the delay is due to the flat region of the waveform while the device is pinched off. Consistent with the experiment,[13] the times for switch-on and switch-off are not equal as shown in the waveform of Figure 11(b). This is because switching-on depends on R_L-C time constant, while switching off depends on r_D-C time constant.

Effects of nonuniform devices and circuit parameter are demonstrated in Figure 12. The waveforms were obtained by random variations of r_D, V_p, and R_L among the inverters. For a maximum variation of 7% of any of the parameters used in describing the five-stage ring oscillator, the delay per stage was 95 ps for TTL as compared to 90 ps in that of Figure 11(b). The waveform became severely distorted when the maximum variation was increased to 70%. As reported,[14] the ring oscillator has a narrower range of lower and upper bias thresholds than theoretical values would indicate. The bias voltage tolerance reduction is apparently due to circuit nonuniformities.

Figure 13 - where it is compared with the experimental result of Ref. (14) - demonstrates that the ring oscillator simulation is realistic. An interconnect capacitance (C_L in Figure 2) value of 0.02 pf and the known characteristic of the 1-μm gate device were used to calculate the delay time vs the power for V_{DD} from 0.6 to 1.6 volts. It is interesting to note that a minimum exists in both curves.

Note also that the small (0.02 pf) interconnect capacitance has a rather drastic effect on the delay time of the enhancement device, which according to Figure 11(a) should have a delay per stage as low as 35 ps. In Figure 13, the delay is about one order of magnitude larger. The enchancement device, due to the lower doping and hence smaller capacitance, is inherently more susceptible to capacitive loading. (The effective time constant of the circuit is apparently $r_D(C+C_L) = \tau(1 + C_L/C)$ where C_L is load capacitance.) However, the enhancement device is capable of achieving a lower Pxt_D product compared to the depletion device because of its higher r_D and smaller logic swing.

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J.R. Eshbach, S.P. Yu, and W.R. Cady, "Avalanche Multiplication in CATTs," Solid State and Electron Devices, 1, 9-16 (1976).

W. Tantraporn and S.P. Yu, "Si Avalanche Memory Triode as a Logic Device," Technical Digest (late news), International Electron Devices Meeting, Washington, DC, 1976.

S.P. Yu and W. Tantraporn "Time-Domain Computer Simulation of Three-Terminal Semiconductor Devices," Proceedings 6th Biennial Cornell Electrical Engineering Conference, 1977.

S.P. Yu and W. Tantraporn, "Dynamic Two-Dimensional Computer Simulation of Three-Terminal Semiconductor Devices," Proceedings European Microwave Conference, Copenhagen, 1977.

S.P. Yu and W. Tantraporn, "Short Gate Effects, Cut-Off Frequence and Switching Delay of the GaAs FET," presented at Workshop on Compound Semiconductor Microwave Material and Devices, San Francisco, 1978.

PERSONNEL

W. Tantraporn and S.P. Yu

INTERACTIONS

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Prof. J. Frey	Cornell University Ithaca, NY
James Skalsky	U.S. Air Force Avionics Lab Dayton, OH

NEW FINDINGS

The single most important dynamic effect of avalanche-generated carriers in the bipolar transistor and transistor-like devices is the feedback of majority carrier through the base. This majority carrier (holes in an n-p-n device) current generates a voltage drop opposite to the normal transistor base current. Under controlled conditions, the hole feedback increases the device g_m and thus f_T. Using this mechanism, a device of a given line resolution can operate at higher frequency or perform faster switching than an equivalent transistor.

Uncontrolled avalanche process in bipolar devices could cause the collector-base junction to behave like a TRAPATT leading to "second breakdown." The initiation of TRAPATT can be effectively inhibited by the use of hyperabrupt collector-base junction such as that used in the CATT or AMT. This doping profile could also be used in the normal transistor not for the purpose of avalanche multiplication as in the CATT, but to prevent the second breakdown. The transistor so designed would not need emitter ballasting.

The avalanche process in GaAs FET could be initiated in the stationary high-field domain which reduces device efficiency. Another more detrimental avalanche is the one that is initiated in the gate-drain depletion region. This process is spontaneous and could spread to the drain and substrate causing device destruction.

The f_T of an FET is determined by an R-C time constant even under velocity saturation. The commonly accepted time constant of gate length divided by carrier saturation velocity is not very useful for this purpose.

The GaAs FET logic device has an intrinsic switching frequency approaching f_T. Since the f_T is independent of doping density, the $P \cdot t_D$ can be reduced by reducing the doping density. However, reducing doping density must be accompanied by reducing the logic swing for optimum operation. Small logic swing imposes a stringent requirement on uniformity in IC processing.

The logic swing and bias thresholds are limited by the variability of device and circuit parameters in an IC. A maximum variation of any of the parameters within 10% should not significantly affect the circuit performance.

In practice the switching speed in an IC depends mainly on the g_m of the device and the load capacitance of the circuit. Poorly designed IC could therefore have a switching speed much slower than the f_T of the active device.

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(2) S.P. Yu and W. Tantraporn, "A New Three-Terminal Microwave Power Amplifier," IEEE Trans. Educ., 21, 736, (1974).

(3) S.P. Yu, W.R. Cady, J.R. Eshbach, and W. Tantraporn, "Hot Hole Effects in Controlled Avalanche Transit-Time Devices," IEEE Trans. Educ., 22, 1066, (1975).

(4) S.P. Yu, W.R. Cady, J.R. Eshbach, and W. Tantraporn, "An S-Band CATT," 5th Biennial Conference on Active Semiconductor Devices, Cornell University, 1975.

(5) S.P. Yu, W. Tantraporn, and J.R. Eshbach, "Theory of a New Three-Terminal Microwave Power Amplifier," IEEE Trans. Educ., 23, 332-343 (1976).

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(8) S.P. Yu and W. Tantraporn, "Dynamic Two-Dimensional Computer Simulation of Three-Terminal Semiconductor Devices," Proceedings European Microwave Conference, 1977.

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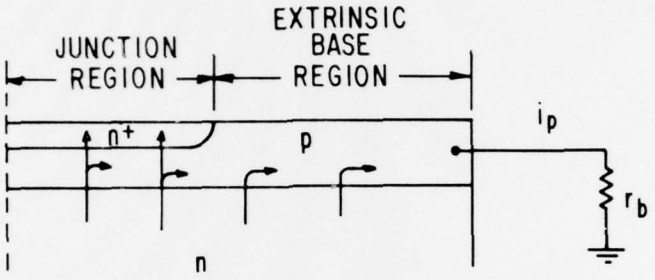


Figure 1. Schematic Representation of the Emitter, Base, and Collector, and the External Resistance. The hole current flow is quantatively indicated by the arrows.

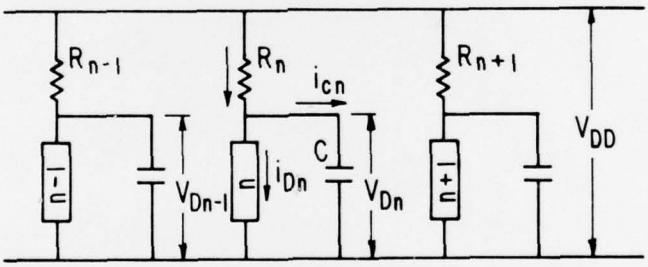


Figure 2. The Equivalent Circuit of a Ring Oscillator, where i_{Dn}, R_n, and C_n Are, Respectively, the Drain Current, Load Resistance and Load Capacitance of the n^{th} Inverter.

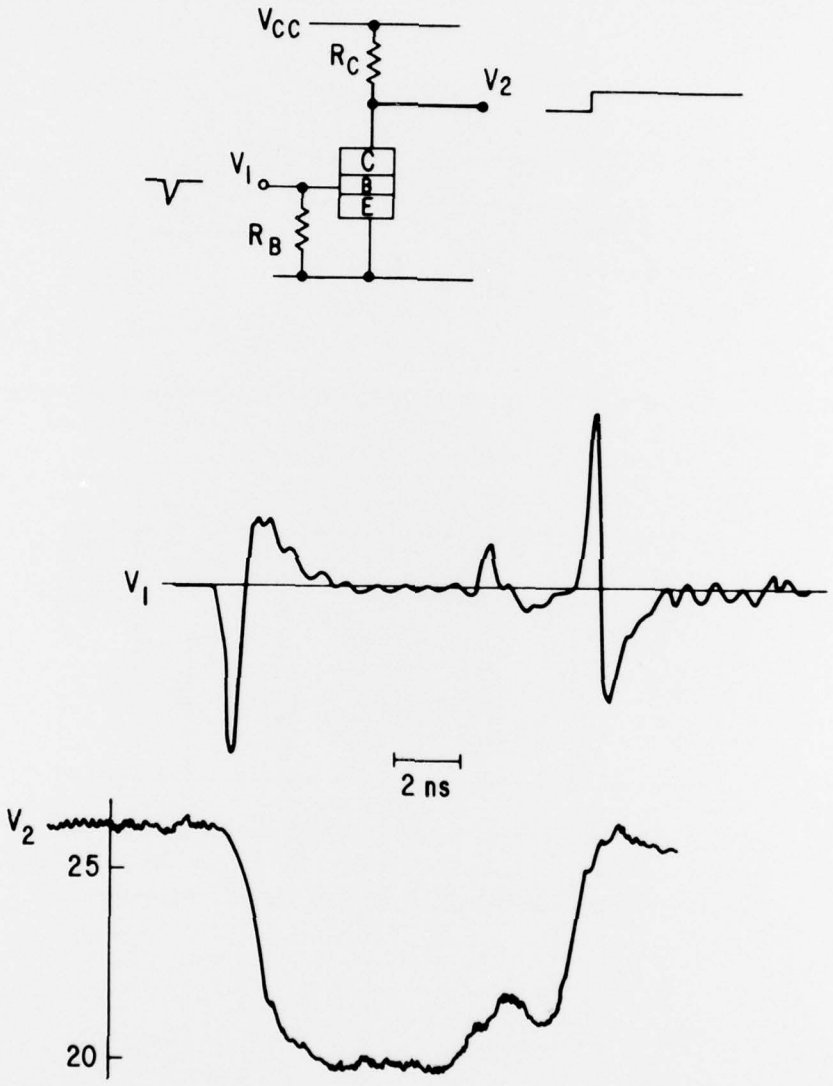


Figure 3. (a) Schematic Representation of the AMT Circuit; (b) a recorder trace of an experimental input waveform V_1; (c) the correspondent output waveform V_2.

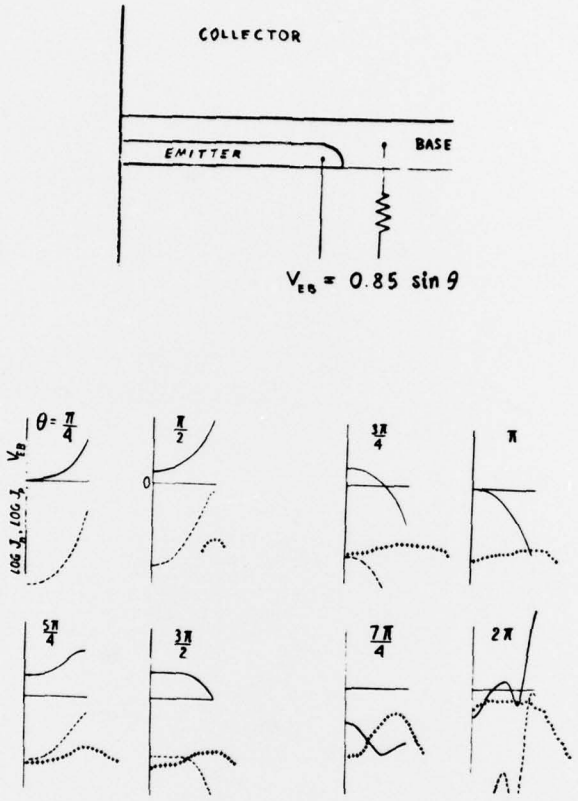


Figure 4. (a) Schematic Representation of the Emitter, Base, and Collector of the AMT. The portion of the base external to the emitter is represented by a sheet resistance. The input voltage is indicated. (b) "snapshots" of the voltage (solid line), electron (-), and hole (+) distributions as a function of the lateral distance from the line of symmetry at various phase angle values. The extent of the emitter is depicted as the horizontal line. The vertical scale unit corresponds to 0.1 V for V_{EB}, and one decade for the electron or hole current density.

Note that the hole current grows as a function of θ. The electron injection follows the voltage. At $\theta = 2\pi$, the emitter is forward-biased due to the hole current despite the fact that the input voltage has returned to zero.

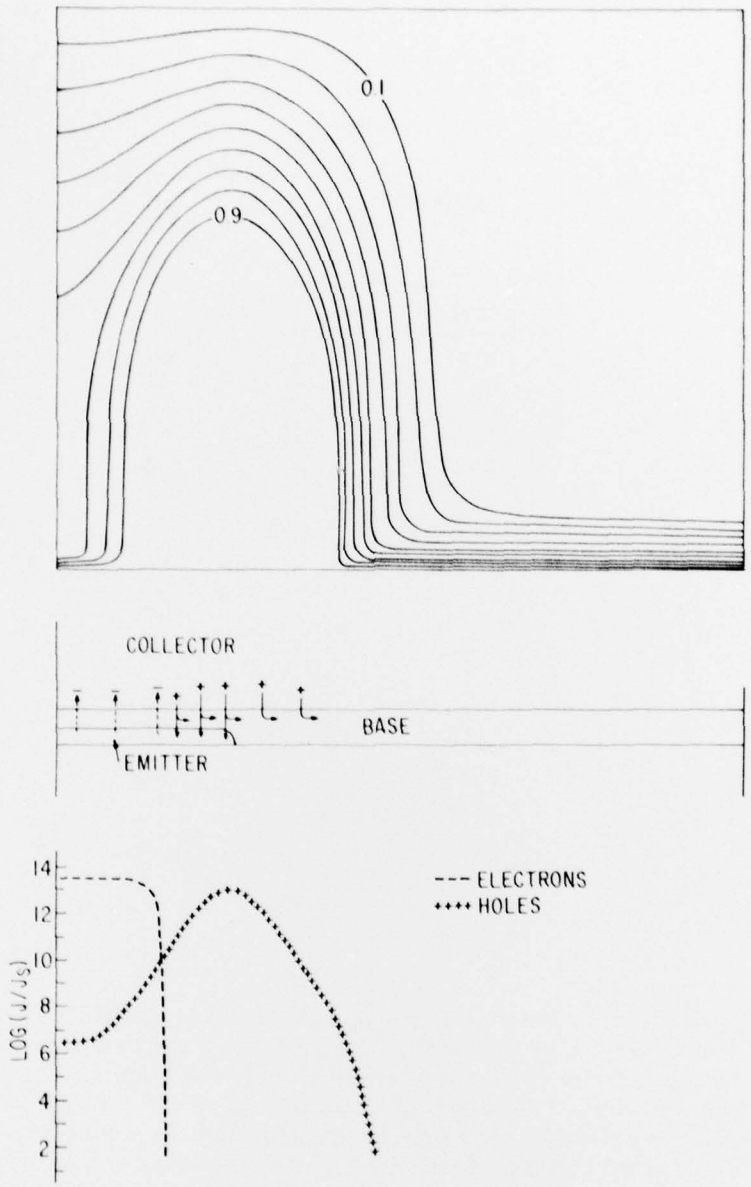


Figure 5. Computer Simulation Result Illustrating the Onset of the "Second Breakdown" when the Device's Hole Current Is Sufficient to Provide Large Forward Bias on the Emitter-Base Junction. Note the pinched-in effect indicated by the electronic injection (--) shown in the lower portion of the figure. The central portion depicts the qualitative processes while the upper portion shows the equipotential contours in the collector space (normalized voltage, high at the base-collector junction and zero at the collector electrode). Note the focusing effect of the potential contours on the hole current (++) and also the crowding of the contour lines in the region remote from the emitter which may lead to subsequent avalanche.

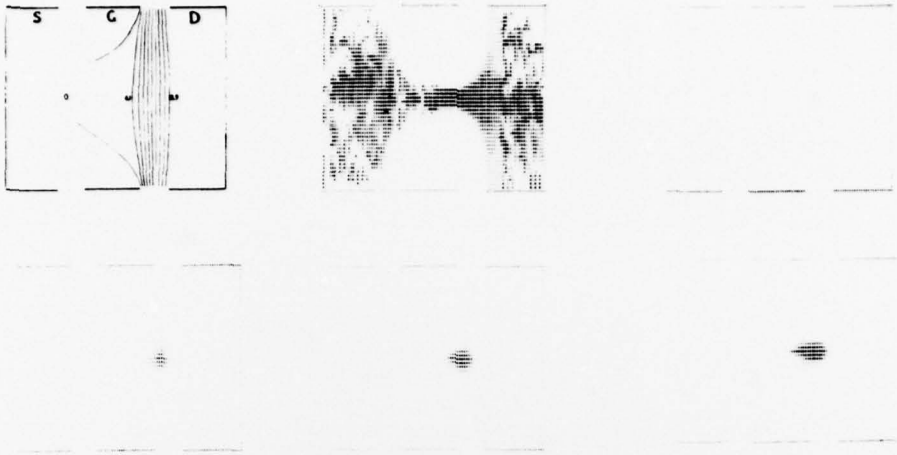


Figure 6. Computer Simulation Result Illustrating Two Regions of Avalanche Multiplication in the MESFET. (The symmetric two-gate structure may be used to represent the normal one-sided gate FET if the lower half is considered as a non-conducting substrate.) The vertical and horizontal scales are not the same; horizontal frame size = 8 μm, vertical = 1 μm. Here $n_D = 10^{16}$ cm^{-3}, L = 2 μm. The drain voltage is $45 \cdot \sin(\theta/2)$ for $\theta \leq \pi$ and remains at 45 V for $\theta \geq \pi$, while $V_{SG} = -2$ V for $\theta \geq 0$; ($2\pi \rightarrow 10^{-10}$ s). The upper three frames depict the potential contour, the electron distribution, and the avalanche-generated holes at time $\theta = 1.885$. The hole distributions at $\theta = 2.12$, 2.36, and 2.59 follow. The grey scale of the hole plotting is 10 times as sensitive as that for the electrons.

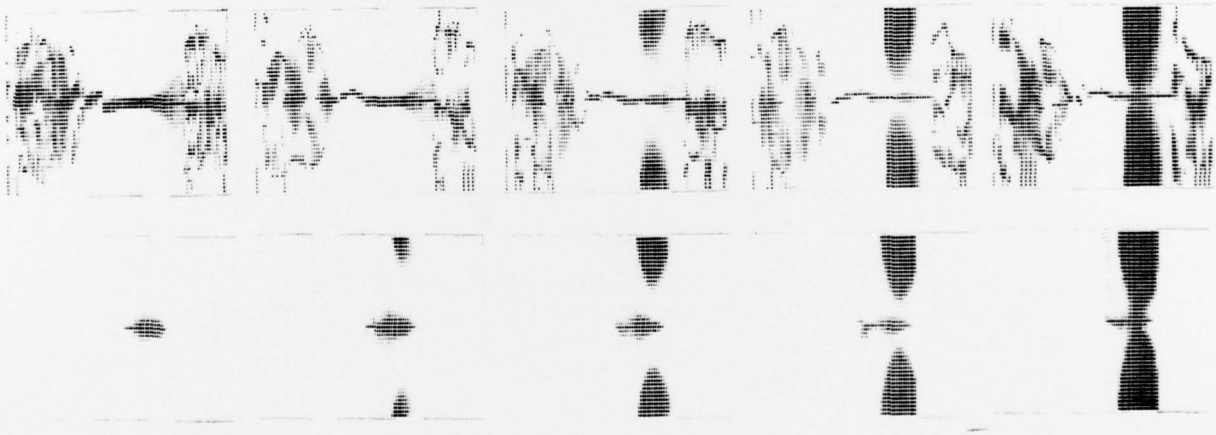


Figure 7. Sequence Continuation of Figure 6 for Both the Electron and Hole Distributions at (from left to right) $\theta = 2.83$, 3.73, 4.20, and 4.59. Again, the grey scale for hole plotting is 10 times as sensitive as for the electron. However, for both the darkest represents "10 or higher", so that only the lighter shades are quantitatively meaningful. At $\theta > 4.65$, computer simulation shows that the avalanche-generated carriers are larger than the background doping everywhere.

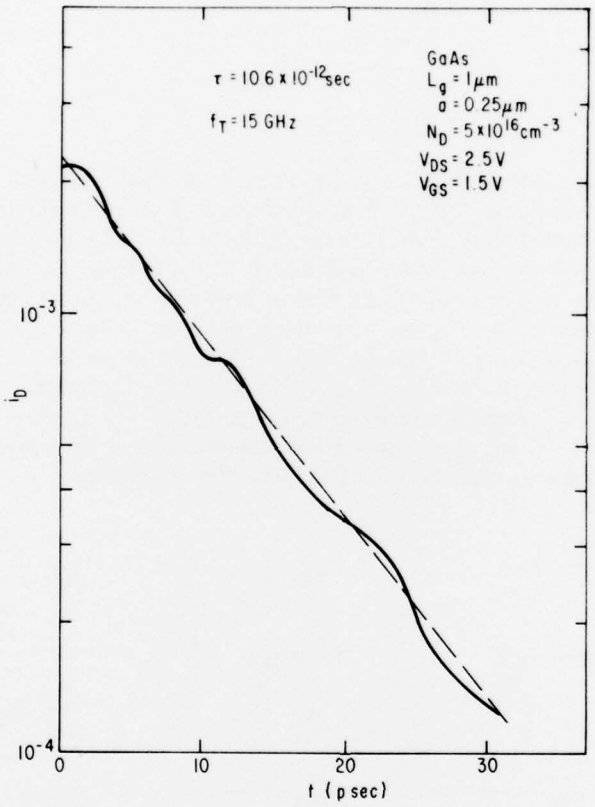


Figure 8. Semilogarithmic Plot of the Drain Current vs Time for a 1 μm Gate GaAs FET. Both the drain and gate voltages are stepwise applied at t=0. The device time constant is determined as the semilogarithmic slope. The cut-off frequency $f_T = 1/2\pi\tau$.

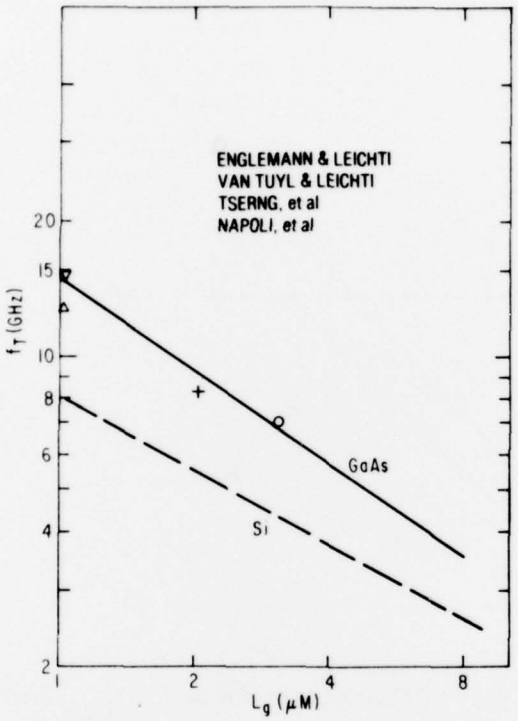


Figure 9. Value f_T Obtained from Computer Simulation Results (see Figure 8) for GaAs and Si as a Function of the Gate Length. Experimental data on GaAs FET are shown for comparison.

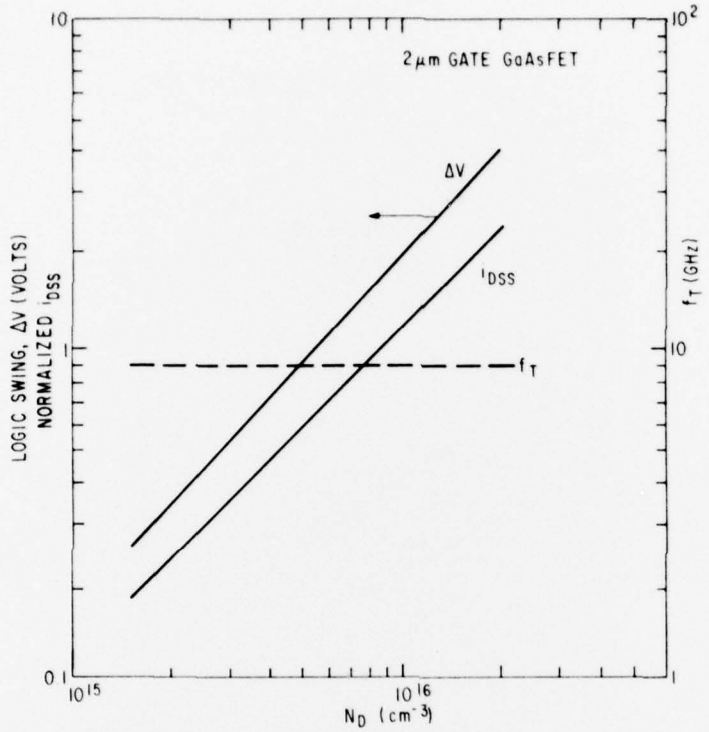
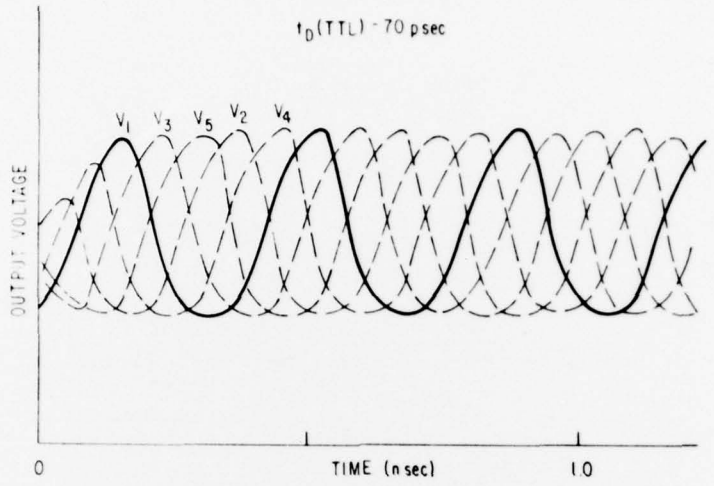
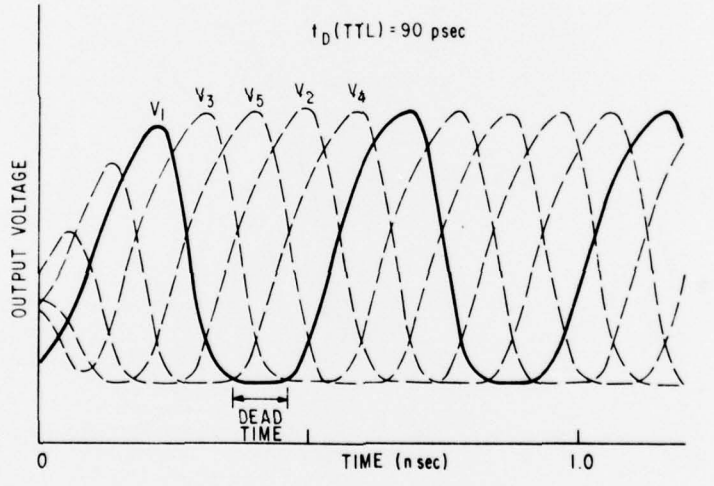


Figure 10. Effect of Doping Density on f_T, i_{DSS}, and Optimum Logic Swing ΔV.

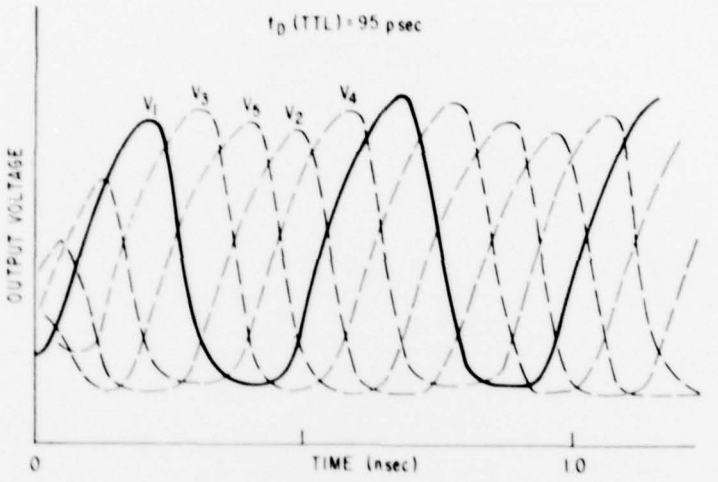


(a)

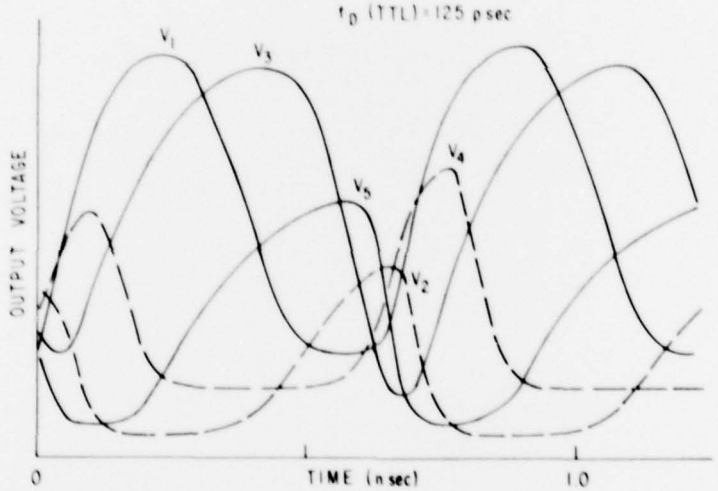


(b)

Figure 11. (a) Voltage Waveform of a Ring Oscillator (consisting of five 1-μm gate inverters) with Circuit Parameters Adjusted for Optimum Swing. The delay per stage is 35 ps, or 70 ps if a TTL configuration is used. (b) voltage waveform of the same ring oscillator when the logic swing is larger than the pinched-off voltage. The time delay per stage is increased due to the dead time region. The simulated waveform with unequal turn-on and turn-off is in agreement with experiments.



(a)



(b)

Figure 12. (a) Slight Nonuniformity (<7%) in the Ring Oscillator Circuit Elements Results in a Slight Increase in the Delay Time and Unequal Voltage Outputs. (b) large nonuniformity (70%) results in greater distortion of the output voltage waveform.

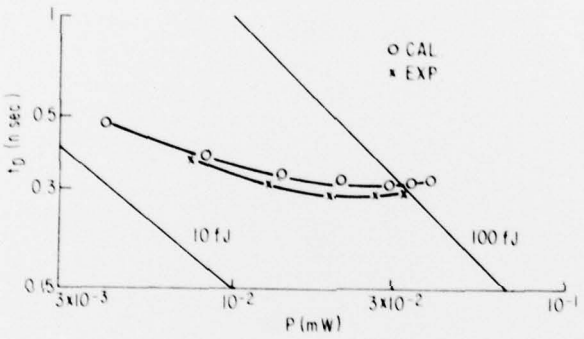


Figure 13. Delay Time vs Power in a Ring Oscillator Consisting of 1 μm Gate Enhancement GaAs FETS. The interconnect capacitance (C_L in Figure 2) of 0.02 pf and the known characteristics of the 1 μm gate FET were used in the calaculation.